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BUS INTERFACE EXTENDER AND METHOD THEREOF

Field of the Invention

The present invention relates to a bus interface extender and a method thereof, and more particularly, to an extender suitable for a PCI bus arbitrator.

Background of the Invention

Peripheral component interconnect (PCI) bus structure is a conventional bus standard published by Intel in 1993. Of the PCI bus devices coupled to a PCI bus, network cards, sound cards and video cards are the norm. In the PCI bus structure, a PCI bus arbiter is typically used to link with several PCI bus devices within a limitation. The PCI bus arbiter plays a role for arbitrating to decide which PCI bus device is granted access to the bus when the PCI bus devices simultaneously need to use a system bus to transmit signals. These signals comprise PCI controlling signals, such as initialization device select signal (IDSEL), request signal (REQ) and grant signal (GNT).

Pins of a conventional PCI bus arbiter can only support a limited number of PCI bus devices and provide fixed functions, and thus cannot be adjusted and modified immediately. When a computer system needs more than a predetermined number of PCI bus devices, another PCI bus arbiter having more pins is needed to make a replacement and the circuit wiring of the circuit board in the computer system needs to be redistributed to meet locations of pins different from these of origin, so the cost is increased. According to the aforementioned description, it will be a work of great

industry worth to design a device that can elastically expand the number of bus devices coupled to the device without modifying the original bus arbiter and the circuit.

Summary of the Invention

Therefore, an objective of the present invention is to provide a bus interface extender and a method thereof, to support more bus devices by cooperating with available bus arbitrators, such as a PCI bus arbitrator.

A bus interface extender in accordance with a preferred embodiment of the present invention is coupled between a bus arbitrator and at least one PCI device. The bus interface extender includes a priority decision module, a grant decision module and a bus signal processing module. The priority decision module determines a priority sequence for each of the bus devices. The grant decision module grants access of the proper bus device to the system bus according to priority and request status thereof. The bus signal processing module manages transmission of request/grant signals between the bus devices and the bus arbitrator according to the decision of the grant decision module.

In addition, a bus interface extending method in accordance with another preferred embodiment of the present invention is applied in a bus architecture; the bus architecture further includes a plurality of first bus devices, a plurality of second bus devices, a bus arbitrator and a bus interface extender. The first bus devices and the extender are coupled to the bus arbitrator, and the second bus devices are coupled to the bus interface extender.

When any of the first bus devices and the second bus devices needs to use a bus, the bus device will send a request signal. Conversely, whichever first bus device or second bus device receives a grant signal first is granted access to use the bus. The

request signal of any first bus device is directly sent to the bus arbitrator for arbitrating, and the request signal of any second bus device is first sent to the bus interface extender for a first arbitration. The arbitration result is transmitted from the bus interface extender to the bus arbitrator for a second arbitration.

When the bus arbitrator receives several request signals simultaneously, the bus arbitrator performs an arbitration step according to a predetermined priority sequence rule and sends a grant signal to the proper first bus device or the proper bus interface extender. When the grant signal is received by the bus interface extender, the bus interface extender transmits the grant signal to the second bus device that has sent a request signal and has high priority according to another predetermined priority sequence rule.

In addition, in order to avoid the same bus device with high priority obtaining grant signals continuously and resulting in a long waiting time for other bus devices, a round-robin priority arbitration mode, for example, can be used according to the priority sequence rule of the bus interface extender of the present invention. The round-robin priority arbitration mode means that the priority sequence of a bus device can be adjusted when the bus device is granted a grant signal.

According the aforementioned description, an advantage of the present invention is that the capability of increasing the number of bus devices coupled thereto is achieved to enhance the flexibility of bus architecture design and take account of the cost concurrently without modifying the architecture of the bus arbitrator.

Brief Description of the Drawings

The advantages and the spirits of the present invention will become better understood by reference to the following detailed description, when taken in

conjunction with the accompanying drawings, where:

FIG. 1 is a diagram illustrating a system architecture of a bus interface extender and a PCI bus arbitrator of the present invention;

FIG. 2 is a diagram illustrating an extender of the present invention;

FIG. 3 is a diagram of a priority table of a fixed-priority arbitration mode in accordance with a first preferred embodiment of the present invention;

FIG. 4A to FIG. 4B are diagrams of a round-robin priority arbitration mode in accordance with a second preferred embodiment of the present invention; and

FIG. 5 is a flow chart showing a bus interface extending method of the present invention.

Detailed Description of the Preferred Embodiment

Referring to FIG. 1, FIG. 1 is a diagram illustrating a system architecture of a bus interface extender 20 and a PCI bus arbitrator 10 in accordance with a preferred embodiment of the present invention. The PCI bus arbitrator 10 works as a PCI signal access device used to arbitrate and control which PCI device coupled thereto can use the bus channel. The PCI bus arbitrator 10 includes a plurality of first pins 101-104 and 131-134 thereon, and the PCI bus arbitrator 10 can be electrically coupled to a plurality of corresponding first PCI devices 105-107 by transmitting lines 108-110 and 148-150, respectively. While the number of PCI devices that can be coupled to the original PCI bus arbitrator 10 needs to be increased, the extender 20 of the present invention can be used to connect electrically extra PCI devices. The extender 20 comprises a plurality of second pin 201-203 and 351-353 in pairs and a pair of third pins 211 and 311. The third pins 211 and 311 are coupled to two first pins 104 and 134 of the PCI bus arbitrator 10 through two transmitting lines 210 and 250, so as to

transmit a request signal or a grant signal. In addition, these second pins 201-203 and 351-353 can be electrically coupled respectively to a plurality of extra second PCI devices 204-206 through transmitting lines 207-209 and 247-249.

FIG. 1 clearly illustrates that although a pair of the first pins 104 and 134 of the PCI bus arbitrator 10 is occupied for coupling the extender 20 and the decrease in the amount of PCI devices that can be coupled to the PCI bus arbitrator 10 is 1, three second PCI devices 204-206 can be additionally coupled to the PCI bus arbitrator 10 though the extender 20 of the present invention to increase the amount of the PCI devices substantially controlled by the PCI bus arbitrator 10 from four to six without redesigning circuit or replacing the original bus arbitrator with one having more pins.

In FIG. 1, each of the first PCI devices 105-107 and the second PCI devices 204-206 is designated as a continuous but unrepeatable PCI device serial number by a system. For example, the PCI device serial numbers of the first PCI device 105, the first PCI device 106 and the first PCI device 107 are designated as 11, 12 and 13, and the PCI device serial numbers of the second PCI device 204, the second PCI device 205 and the second PCI device 206 are designated as 21, 22 and 23, as shown in the table of FIG. 3. In the system bus, these first and second PCI devices may be respectively in one of two conditions, request status and un-request status. The request status means that if any of the first or second PCI devices has a bus signal to be transmitted, it will send a request signal to ask for a formation of bus channel.

Further referring to FIG. 2, FIG. 2 is a diagram illustrating an extender 20 in accordance with a preferred embodiment of the present invention. The extender 20 mainly comprises a priority decision module 301, a grant decision module 302 and a PCI signal processing module 303. The priority decision module 301 sets a priority sequence (such as a priority table illustrated in FIG. 3) for each of the second bus

devices 204-206 according to a priority decision rule 304. The priority decision rule 304 is used to decide the priority sequence for the second bus devices 204-206 to obtain the system bus controlling priority. The grant decision module 302 is used to determine the second PCI device with highest priority between these second PCI devices 204-206, and to confirm that it is the second PCI device with the highest priority in request status, when the system is initialized. The PCI signal processing module 303 is used to manage transmission of request/grant signals between the second PCI devices 204-206 and the PCI bus arbitrator 10.

Therefore, when any of second PCI devices 204-206 sends a second request signal through the transmitting line thereof to the extender 20 for an access to the bus channel, the PCI signal processing module 303 correspondingly sends a first request signal through the third pin 211 to the PCI bus arbitrator 10, and the first request signal together with the request signals sent from the first PCI devices 105-107 are arbitrated.

Subsequently, when another third pin 311 of the extender 20 receives a first grant signal transmitted from the PCI bus arbitrator 10 after arbitrating, the PCI signal processing module 303 correspondingly sends a second grant signal to the proper second PCI device and grants access of controlling right of the system bus to the proper second PCI device, so as to form the bus signal transmission between the proper second PCI device and the system bus, according to the decision of the priority sequence and request status to each of the second PCI devices 204-206 (to be described later).

It should be noted that said priority decision module 301, said grant decision module 302 and said PCI signal processing module 303 can be attained by executing circuit logic or using a controller with software or firmware. Furthermore, the priority table illustrated in FIG. 3 can be recorded in a storage medium, such as a memory, for

example, a flash memory.

Referring to FIG. 3, FIG. 3 is a diagram of a priority table of a fixed-priority arbitration mode adapted in a priority decision rule 304 of an extender 20 in accordance with a first preferred embodiment of the present invention. The aforementioned priority table lists the corresponding PCI device serial number and the corresponding priority number of each of the second PCI device 204-206. The larger the PCI device serial number is, the higher the priority number is, i.e. the lower the priority sequence is. The priority sequence in the fixed-priority arbitration mode does not change, always preserving the priority of the PCI device having the PCI device serial number of 21 as the highest, the priority of the second PCI device having the PCI device serial number of 22 as the next highest, and the priority of the PCI device having the PCI device serial number of 23 as the lowest, as shown in FIG. 3.

In the first embodiment of the present invention, when the PCI signal processing module 303 of the extender 20 in FIG. 1 and FIG. 2 receives a first grant signal transmitted from the PCI bus arbitrator 10, the grant decision module 302 searches the second PCI devices 204-206 for the second PCI device with highest priority, such as the second PCI device 204 with the priority number of 1 listed in the priority table in FIG. 3, according to the priority sequence predetermined in the priority decision rule. When the PCI signal processing module 303 decides that the second PCI device 204 is not in request status, i.e. the second PCI device 204 has not sent a request signal to the extender 20 for the bus channel before, the grant decision module 302 searches for the second PCI device 205 with the second high priority (priority number is 2) according to the priority table, and simultaneously finds that the second PCI device 205 is in request status, which represents that the second PCI device 205 has sent a request signal to the PCI bus arbitrator 10 through the extender 20. The grant decision module 302 sends a

second grant signal with a bus controlling right to the second PCI device 205 through the PCI signal processing module 303 to grant access by connecting the second PCI device 205 and the system bus, so as to perform PCI bus signal transaction. In contrast, if the second PCI device 205 is not in request status, the grant decision module 302 continuously searches for the second PCI device 206 with the priority number of 3 and makes a decision, and so on, to accomplish the work of arbitrating.

However, when the fixed-priority arbitration mode is adapted in the priority decision rule 304, the PCI device with higher priority usually occupies the bus controlling right. This means that if the second PCI device 204 with the highest priority is continuously in request status, all the bus controlling rights will be occupied by the second PCI device 204.

Therefore, according to a second embodiment of the present invention, the priority decision rule 304 of the extender 20 adapts a round-robin priority arbitration mode. Referring to FIG. 4A to FIG. 4B, FIG. 4A to FIG. 4B are diagrams illustrating a priority table of a round-robin priority arbitration mode adapted in the priority decision rule 304 in accordance with a second preferred embodiment of the present invention. At initialization, the priority table of the round-robin priority arbitration mode is similar to that in the first embodiment; the larger the PCI device serial number is, the lower the priority sequence is. The difference between the first embodiment and the second embodiment is that after the second PCI device with highest priority sequence obtains a first grant signal sent by the PCI bus arbitrator 10 through the extender 20, the priority of the second PCI device with highest priority sequence is lowered. In other words, the priority sequence granted to each of the second PCI devices 204-206 is changed but fixed for each arbitration. For example, on the first (or initial) arbitration illustrated in FIG. 3, the priority of the second PCI device 204 with PCI device serial

number 21 is originally the highest. After the second PCI device 204 once obtains a grant signal, the priority of the second PCI device 204 becomes the lowest priority 3 shown in FIG. 4A, the priority of the second PCI device 205 with PCI device serial number 22 of the second highest shown in FIG. 3 becomes to the highest with highest priority number 1 shown in FIG. 4A on the second arbitration. At this time, the second PCI device 205 with the PCI device serial number 22 having the highest priority does not make a request, while the second PCI device 206 with the PCI device serial number 23 makes a request, so the second PCI device 206 receives a second grant signal sent by the PCI bus arbitrator 10 through the extender 20. After the second PCI device 206 has used the bus channel, the priority number of the second PCI device 206 with the PCI device serial number 23 becomes the lowest of 3, while the priority number of the second PCI device 205 with the PCI device serial number 22 remains 1 because the second PCI device 205 never transmits a PCI signal.

Further referring to FIG. 5, FIG. 5 is a flow chart showing a bus interface extending method in accordance with the present invention. The steps in the method are described below. First, in step S30, the system starts at an initial condition. Next, in step S31, any of the second PCI devices 204-206 sends a second request signal to the extender 20. Then, in step S32, the extender 20 correspondingly sends a first request signal to the PCI bus arbitrator 10 according to the received second request signal. After step S32, step S 33 is performed, and the PCI bus arbitrator 10 arbitrates the first request signal and the other request signals sent by the first PCI devices 105-107 to decide whether the first request signal is granted. If the result of the decision is "no", the arbitration result represents that the request signals sent by the first PCI devices 105-107 are granted. The process then proceeds to step S34, and the PCI bus arbitrator 10 sends a first grant signal to the granted first PCI device. On the contrary, if the

result of the decision is "yes", the arbitration result represents that the first request signal sent by the extender 20 is granted. The process then proceeds to step S41, and the extender 20 receives a first grant signal sent by the PCI bus arbitrator 10. Next, step S42 is performed to decide the priority sequence of the second PCI devices 204-206 according to a specific priority decision rule. Subsequently, step S43 is performed to find the second PCI device with the highest priority. Then, step S44 is performed to confirm whether the found second PCI device is in status of requesting use of the bus.

If the result of the decision in step S44 is "yes", step S45 is performed to correspondingly send a second grant signal to the second PCI device which is found and then step S47 is performed. On the contrary, if the result of the decision is "no", the process proceeds to step S46 to search the next second PCI device with the second highest priority according to a specific priority decision rule, and then the process returns to step S44 to decide once more whether the second PCI device with the second high priority is in status of requesting use of the bus. If the result of the decision is still "no", then a second PCI device with a lower priority is decided, and so on. When a second PCI device in status of requesting use of the bus is finally found and each of the other second PCI devices with the higher priority does not make a request, the process proceeds to step S45 to send a second grant signal to the second PCI device which is found, so as to grant the found second PCI device the controlling right of the system bus channel. Then, step S47 is performed to form the transmission channel of the bus signal between the second PCI device and the system bus. Subsequently, if any second PCI device makes a request, the process returns to step S31.

The priority calculation of the extender of the present invention is not limited to the aforementioned fixed-priority arbitration mode calculation and the round-robin priority arbitration mode calculation, so the extender of the present invention can be

coupled with a conventional PCI bus arbitrator. Therefore, the amount of PCI devices that can be controlled by the conventional PCI bus arbitrator can be increased without redesigning the circuit or using another PCI bus arbitrator having more pins to replace the original one.

As is understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrated of the present invention rather than limiting of the present invention. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structure.